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SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND METHOD FOR MAKING SAME

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SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND FABRICATION PROCESS

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The present invention relates in general to a semiconductor device, such as an MOS transistor, in which there is compensation for the drop in the threshold voltage (V_{th}) due to the short channel effects, and to a process for fabrication such a semiconductor device.

For a given nominal channel length (L) of a transistor, the threshold voltage (V_{th}), in particular for short-channel transistors, that is to say those having a channel length of less than 0.25 μm and typically a channel length L of about 0.18 μm, drops suddenly.

The threshold voltage of a semiconductor device such as an MOS transistor, in particular a short-channel device, is a critical parameter of the device. This is because the leakage current of the device, for example, of the transistor, depends strongly on this threshold voltage. Taking into consideration the current supply voltages and those envisaged in the future (from 0.9 to 1.8 volts) for such devices and the permitted leakage currents (I_{off} of approximately 1 nA/μm), the threshold voltage V_{th} must have values of approximately 0.2 to 0.25 volts.

The sudden voltage drop (or roll-off) in the zones of the channel region of the semiconductor device results in dispersion of the electrical characteristics of the device and makes it difficult to obtain the desired threshold voltages.

To remedy this threshold voltage roll-off in semiconductor devices such as MOS transistors, it has been proposed, as described in the article "*Self-Aligned Control of Threshold Voltages in Sub-0 .2-μm MOSFETs*" by Hajima Kurata and Toshihiro Sugii, IEEE Transactions on Electron Devices, Vol. 45, No. 10, October 1998, to form, in the channel region, pockets adjacent to the source and drain region junctions and having a conductivity of the same type as the substrate, but the dopant concentration of which is greater than that of the substrate.

Although this solution reduces the threshold voltage roll-off gradient in the channel region, the short-channel effects lead to a more rapid roll-off of the threshold voltage V_{th} than the increase in the threshold voltage that can be obtained by incorporating the compensation pockets of the prior art.

Consequently, although these compensation pockets of the prior art allow partial local compensation for the roll-off of the threshold voltage V_{th}, it is thus not possible to obtain complete compensation for the roll-off over the entire channel region range desired.

The subject of the present invention is therefore a semiconductor device, such as an MOS transistor, which remedies the drawbacks of the devices of the prior art.

The subject of the present invention is more particularly a semiconductor device, such as an MOS transistor, whose voltage threshold roll-off due to the short-channel effects is almost fully compensated for, making it possible to achieve channel lengths which are arbitrarily small but non-zero.

The subject of the present invention is also a semiconductor device, such as an MOS transistor, having a constant threshold voltage V_{th} when the channel length L decreases down to very small effective channel lengths, for example 0.025 μm or less.

The subject of the present invention is also a process for fabricating a semiconductor device as defined above. This process may apply to devices having channels of arbitrarily small length, these being, moreover, technologically realizable.

The above objectives, according to the invention are achieved by fabricating a semiconductor device comprising a semiconductor substrate having a predetermined concentration Ns of a dopant of a first conductivity type, source and drain regions which are doped with a dopant of a second conductivity type, the opposite of the first, and define, in the substrate, junctions delimiting a channel region of predetermined nominal length L_N, and, in the channel region, a first pocket adjacent to each of the junctions and

having a predetermined length Lp, said first pockets being doped with a dopant of the first conductivity type but with a local concentration Np locally increasing the net concentration in the substrate, this device being characterized by the presence of at least one second pocket adjacent to each of the junctions and stacked against each of the first pockets, these second pockets having a length Ln such that Ln > Lp and being doped with a dopant of the second conductivity type with a concentration Nn such that Nn < Np locally decreasing the net concentration of the substrate but without changing the conductivity type.

According to a preferred embodiment of the invention, the second pockets comprise a plurality of elementary pockets stacked against one another, each elementary pocket of a given rank i having a predetermined length Ln_i and a predetermined concentration Nn_i of a dopant of the second conductivity type satisfying the following relationships:

$Ln_1 > Lp$

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} > Nn_i > Nn_{i+1}$, and

the sum ΣNn_i of the concentrations of the dopant of the second conductivity type in the elementary pockets being such that:

$\Sigma Nn_i < Ns$.

In other words, the second pockets decrease the net concentration of dopant of the first conductivity type both in the first pockets and in the channel region, but do not change the conductivity type of the first pockets nor of the channel region.

The present invention also relates to a process for fabricating a semiconductor device as defined above which comprises the formation, in a semiconductor substrate having a predetermined concentration Ns of a dopant of a first conductivity type, of a source region and of a drain region which are doped with a dopant of a second conductivity type, the opposite of the first, the source and drain regions forming, in the substrate, junctions delimiting between them a channel region having a predetermined nominal length L_N, and the formation, in the channel region in a zone adjacent to each of the junctions, of a

first pocket having a predetermined length Lp and a predetermined concentration Np locally increasing the net concentration in the substrate above Ns, the process being characterized in that it furthermore comprises the implantation, in the channel region, of a dopant of the second conductivity type, the opposite of the first, under conditions such that at least one second pocket is formed in the channel region, this second pocket being stacked against each of the first pockets respectively, and having a length Ln such that Ln > Lp and a concentration Nn of a dopant of the first type such that Nn < Np and locally decreasing the net concentration in the substrate, but without changing the conductivity type.

In a preferred embodiment of the process of the invention, the implantation of the dopant of the second conductivity type consists of a series of successive implantations under conditions such that the second pockets formed each consist of a plurality of elementary pockets stacked against one another, each elementary pocket of a given rank i having a length Ln_i and a concentration Nn_i of a dopant of the second conductivity type satisfying the relationships:

$Ln_1 > Lp$

$Ln_{i-1} < Ln_i < Ln_{i+1}$

$Nn_{i-1} > Nn_i > Nn_{i+1}$ and

the sum ΣNn_i of the concentrations of the dopant of the second conductivity type in the elementary pockets being such that:

$\Sigma Nn_i < Ns$.

The lengths Lp and Ln of the pockets are taken from the junctions.

Implantation of a dopant in a semiconductor substrate is a known process and it is possible, in the present process, to use any implantation process conventionally used in the technology of semiconductors.

As is known, the formation of doped pockets in a semiconductor substrate depends on the angle of incidence of the implantation with respect to the normal to the substrate, on the

implantation dose and on the implantation energy of the dopant. Thus, by varying the angle of incidence and the dopant dose, it is possible to increase the length of the implanted pocket and to vary the dopant concentration.

As a variant, in order to vary the length of the second implanted pockets and their dopant concentration, successive implantations may be carried out with the same angle of incidence with respect to the normal, the same dose and the same implantation energy but by subjecting the device after each successive implantation to an annealing heat treatment so as to make the dopant implanted in the substrate diffuse differently.

The remainder of the description refers to the appended figures, which show respectively:

- figure 1, a first embodiment of a semiconductor device, such as an MOS transistor, according to the invention;
- figure 2, a second embodiment of a semiconductor device according to the invention; and
- figure 3, a graph of the threshold voltage (V_{th}) for various semiconductor devices according to the invention as a function of the effective channel length.

Figure 1 shows a first embodiment of a semiconductor device according to the invention, such as an MOS transistor, comprising, as is conventional, a semiconductor substrate 1, for example a silicon substrate doped with a dopant of a first conductivity type, for example p-type conductivity, in which are formed source 2 and drain 3 regions doped with a dopant of a second conductivity type, the opposite of the first, for example an n-type dopant, which in the substrate define junctions 4, 5 delimiting between them a channel region 6.

As is known, the channel region 6 is covered with a gate oxide layer 11, for example a thin silicon oxide layer, which is itself surmounted by a gate 12, for example made of silicon. As is also well known, the gate 12 may be flanked on two opposed sides by spacers 13, 14 made of a suitable dielectric.

As is known, to reduce the rate of roll-off of the threshold voltage V_{th} in the channel region 6, two first pockets 7, 8 are formed in the channel region, each being adjacent to one of the junctions 4, 5 respectively. These pockets are doped by means of a dopant of the first conductivity type p, but with a concentration Np of dopant of the first type which locally increases the concentration in the substrate to above Ns and has a length Lp as short as possible.

According to the invention, two second pockets 9, 10 are formed in the channel region 6, which second pockets are each stacked against one of the first pockets, but with a length Ln greater than the length Lp of the first pockets, and are doped with a dopant of the second conductivity type, for example an n-type dopant, with a concentration Nn such that Nn is less than the concentration Np of dopant of the first conductivity type in the substrate.

Thus, in the zones of the second pockets, the net concentration of dopant of the first conductivity type, for example the p-type dopant, is decreased but the nature of the conductivity in the channel region is not changed, the channel still remaining a region of p-type conductivity.

Figure 2, in which the same reference numbers denote the same elements as previously, shows another embodiment of a semiconductor device according to the invention which differs from the previous device shown in figure 1 only by the fact that the second pockets 9, 10 consist in fact of pluralities of elementary pockets stacked against one another - three elementary pockets in the embodiment shown in figure 2.

Each elementary pocket of a given rank i has a length Ln_i and a concentration Nn_i of dopant of the second conductivity type which satisfy the following relationships:

$$Lp < Ln_i$$

$$Ln_{i-1} < Ln_i < Ln_{i+1}$$

$$Nn_{i-1} < Nn_i < Nn_{i+1}, \text{ and}$$

the sum ΣNn_i of the concentrations of dopant of the second conductivity type in the elementary pockets being such that:

$$\Sigma Nn_i < Ns.$$

In other words, the elementary pockets stacked against the first pockets 7 and 8 are also stacked against one another, but they have increasing lengths and, concurrently, concentrations of dopant of the first conductivity type which decrease as their lengths increase.

Moreover, the sum of the concentrations ΣNn_i of the stacked elementary pockets is such that it remains less than the concentration Ns of dopant of the first conductivity type in the substrate so that the conductivity type of the channel region 6 is not modified.

Thus, in the case shown in figure 2, in which the second pockets consist of three elementary pockets, the lengths and dopant concentrations of the elementary pockets satisfy the relationships:

$$Lp < Ln_1$$

$$Ln_1 < Ln_2 < Ln_3$$

$$Nn_1 > Nn_2 > Nn_3 \text{ and}$$

$$Nn_1 + Nn_2 + Nn_3 < Ns.$$

Figure 3 shows simulated graphs of the threshold voltage V_{th} for transistors having a gate oxide layer 4 nm in thickness and for a drain/source voltage of 1.5 volts as a function of the effective channel length. The lengths Lp and the concentrations Np of the first pockets doped with a dopant of the same type as the substrate correspond to the minimum channel length to be obtained and the highest doping.

Curve A corresponds to the stacking of a single second pocket according to the invention and shows that a flat V_{th} is obtained for a channel length down to 0.15 μm.

Curve B corresponds to the stacking of two second pockets according to the invention and shows that a flat V_{th} is obtained for a channel length down to 0.07 μm.

Finally, curve C corresponds to the stacking of seven second pockets according to the invention and shows that a flat V_{th} can be obtained for a channel length down to 0.025 μm.

Thus, the above curves show that the necessary doping levels remain reasonable and make it possible to obtain flat curves of V_{th} as a function of the effective channel length down to effective lengths of 25 nm, this being so even with gate oxide thicknesses of 4 nm.